EV355228705

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Phase Synchronization For Wide Area Integrated Circuits

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ATTORNEY'S DOCKET NO. RB1-045US

TECHNICAL FIELD

The invention relates to clock signal synchronization in integrated circuits.

BACKGROUND

Integrated circuits (IC), including application specific integrated circuits (ASIC), are increasing in processing capability and are shrinking in physical size. Smaller ICs contain added components such as digital receiving and processing devices. Decreasing the size of ICs has led to an increase in IC processing speed since communication paths are decreased between IC components.

As IC size decreases, however, resistance-capacitance (RC) time delay of metal interconnects between IC components begins to limit IC performance. Interconnect RC time delay is associated with metal resistance of interconnections and capacitance associated with dielectric media. Because metal resistance and dielectric media are inherently part of the materials used in construction of an IC, only a change in materials will affect (improve) RC time delay. A change in materials may be technically impossible or cost prohibitive.

Differences in propagation delay, when compounded across all interconnections, such as clock nets or paths, in a complex IC may lead to unacceptable degradations in overall system-timing. This problem is often referred to as "clock skew."

Fig. 1 illustrates a clock tree that distributes clock signals in a controlled manner. An IC may contain numerous clocked components requiring clock signals. A clock tree or similar clock architecture provides the necessary clock signals to the components. Components within an IC, specifically registers of the components, may require that the clock signals be synchronized. To be considered

"synchronized," clock signals have the same phase at different receivers, despite propagation delays.

In this particular example, clock receiving components 10, 15, 20, and 25 reside on a single IC. Components 10, 15, 20, and 25 may be at varying distances from one another. In other words component 10 may be an unequal distance from component 15, as component 15 is to component 20. Oftentimes, due to IC design constraints or physical architecture restrictions on an IC, components must be placed at varying locations at varying distances from one another. In this example, components 10, 15, 20, and 25 are components that must be synchronized with one another (i.e. have the same phase clock signals). Further, since components are placed at varying distances from one another, components may also be located at varying distances from a clock source such as clock driver 30. Since clock signals travel over varying distances from the clock source to the components, assuring that each clock signal is in phase with the other clock signals becomes a complicated task.

In typical clock architectures such as the clock tree of Fig. 1, a controller such as controller 35 initiates a clock signal. Controller 35 can be located on an IC (on-chip) or external to an IC (off-chip). Controller 35 instructs clock driver 30 to generate a clock signal. Clock driver 30 may be implemented for example as a clock oscillator or clock generator or similar component. Alternatively, clock driver 30 may be a clock buffer. A clock signal transmitted by clock driver 35 is passed on to fan-out clock drivers 40, 45, 50, 55, 60, and 65. All clock signals derived from clock driver 30 have the same frequency, although clock signals arriving at various components or registers may have different phase values.

To assure that the clock signals arriving at components 10, 15, 20, and 25 are properly synchronized and have the same phase, paths 70, 75, 80, and 85 must have approximately the same length and propagation delay characteristics. If components 10, 15, 20, and 25 are not located equidistant from their respective clock drivers 50, 55, 60, and 65, certain paths may have to be wrapped around to assure equal lengths and propagation characteristics of all paths. When IC space is at a premium, this approach may not be feasible.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a clock tree diagram in accordance of the prior art.

Fig. 2 is a schematic illustrating component synchronization for multiple registers in an IC.

Fig. 3 is a schematic illustrating a phase feedback element that makes use of a phase comparator and clock skew register.

Fig. 4 is a schematic illustrating a phase feedback element that makes use of matched current sources.

DETAILED DESCRIPTION

Fig. 2 illustrates a circuit having registers that are to be synchronously clocked. Specifically, this circuit has a plurality of components 200, 205, and 210. In this example, each component comprises one or more multi-bit or byte-word registers. Each byte-word register might have eight individual bit registers, as shown, or some other number of bit registers, typically from 8 to 16 bit registers. In certain other embodiments, all bit registers might be treated as separate registers.

In Fig. 2, component 200 is made up of bit registers 200A-H. Component 205 is made up of bit registers 205A-H. Component 210 is made up of bit registers 210A-H. In this example, bit registers 200A-H, 205A-H, and 210A-H make up a continuous string of bit registers. In other words, bit registers 200A-H, 205A-H, and 210A-H are physically laid out contiguous to one another (side by side). Bit registers 200A-H, 205A-H, and 210A-H may be arranged in a particular sequence. For example, for a pair of components, the last bit register of a first component may be located adjacent the first bit register of a second component. Therefore, bit register 200H is placed directly adjacent to bit register 205A, and bit register 205H is placed directly adjacent to bit register 210A. Logically, however, bit registers 200A-H, 205A-H, and 210A-H are configured to comprise separate components (i.e., they are logically part of components 200, 205, and 210). As separate components, bit registers 200A-H, 205A-H, and 210A-H receive separate component clock signals.

Components 200, 205, and 210 and their respective bit registers are intended to be synchronized with one another. In other words, these components are intended to be synchronously clocked. To achieve this, component clock signals to each byte-word register are adjusted to have matching phases at the byte-word registers, after accounting for any differing propagation delays of the component clock signals. A factor determining propagation delay difference is the difference between the lengths of the paths. In a preferred embodiment, the difference between propagation delays is less than 15%.

The described embodiment includes a clock driver corresponding to each set of components, which in this case equates to a separate clock driver for each respective byte-word register. Thus, a clock driver 215 provides a component

clock signal 218 to bit registers 200A-H of component 200. Component clock signal 218 travels along a path 219 from clock driver 215. Path 219 branches out to sub-paths 219A-H which lead to individual bit registers 200A-H, respectively. Clock driver 220 provides a component clock signal 222 to bit registers 205A-H of component 205. Component clock signal 222 travels along a path 224 from clock driver 220. Path 224 branches out to sub-paths 224A-H which lead to individual bit registers 205A-H, respectively. Clock driver 225 provides a component clock signal 227 to bit registers 210A-H of component 210. Component clock signal 227 travels along a path 229 from clock driver 225. Path 229 branches out to sub-paths 229A-H which lead to individual bit registers 210A-H, respectively. Therefore, the clock drivers 215, 220, and 225 provide separate clock signals to each of the bit registers 200A-H, 205A-H, and 210A-H by way of separate paths.

Clock driver 215, 220, and 225 may receive input clock signals from a common source such as a clock tree. Such a clock tree architecture may be part of the same IC in which components 200, 205, and 210 reside or may be part of another IC.

In this example, a master clock driver 230 produces a common clock signal 232 that branches out to clock drivers 215, 220, and 225. Since clock drivers 215, 220, and 225 derive respective component clock signals 218, 222, and 227 from common clock signal 232, each of the component clock signals is a variably-delayed version of common clock signal 232.

Since component clock signals 218, 222, and 227 originate from a common clock signal source, they have the same frequency. However, as component clock signals 218, 222, and 227 travel across respective paths 219, 224, 229, and the

sub-paths leading to individual bit registers, component clock signals 218, 222, and 227 traverse potentially different distances. Different distances result in differing propagation delays, which result in component clock signals that are potentially out of phase with each other as they are received at the respective components 200, 205, and 210. Clock drivers 215, 220, and 225 are capable of varying the phase of component clock signals 218, 222, and 227 so that the phases of the component clock signals 218, 222, and 227 are synchronized upon arrival at the bit registers of components 200, 205, and 210.

A reference clock signal 240 is used to correct the phases of component clock signals 218, 222, and 227, so that they are in phase with each other at the physical locations of the byte-word registers 210, 215, and 220. Reference clock signal 240 has the same frequency as clock signals 218, 222, and 227. Reference clock signal 240 may be generated by an arbitrary clock source; however, it is contemplated that reference clock signal 240 may be provided by or derived from the same clock tree or clock architecture from which component clock signals 218, 222, and 227 are derived. In certain cases, one of clock signals 218, 222, and 227 may be branched and used as reference clock signal 240. It is not necessary for reference clock signal 240 to have any particular phase relationship with the component clock signals 218, 222, and 227, although its phase preferably remains constant over time as compared to the component clock signals.

The circuit of Fig. 2 has a reference feedback element 250 that receives component clock signal 218 from path 252. Path 252 is a continuation of one of the sub-paths 219A-H and originates from near register 200. In this example, path 252 is connected to path 219D. Reference clock signal 240 travels along path 254 to reference phase feedback element 250. Reference phase feedback element 250

compares the phases of component clock signal 218 and reference clock signal 240, and provides an adjustment signal 251 to clock driver 215. Adjustment signal 257 represents an advance or delay value that allows component clock signal 218 to become in phase with reference clock signal 240. An adjusted component clock signal 218 may then be used as a reference clock signal for other component clock signals. In other words, when the components are considered in sequence, the component clock signal to any particular component is matched in phase to the component clock signal of the immediately preceding component in the sequence.

Note that in certain embodiments, reference clock signal 240 may not be used. In this case, the component clock signals of the components are simply synchronized to that of the first component in the sequence.

In addition to reference phase feedback element 250, the circuit includes phase feedback elements 255 and 260 corresponding to adjacent pairs of components. The phase feedback element corresponding to a particular pair of components receives the component clock signal from a register of each of the components of the particular pair. The component clock signal in each case is routed from a point physically near its corresponding register (of the corresponding component). The phase feedback element is responsive to the received component clock signals to adjust the phase of one of the component clock signals to match the phase of the other component clock signal. More particularly, each phase feedback element receives a first component clock signal from a particular register and a second component clock signal from an immediately subsequent register in sequence, and adjusts the second component clock signal to match the phase of the first component clock signal.

With specific reference to Fig. 2, phase feedback element 255 receives component clock signal 218 from path 256, and component clock signal 222 from path 257. Path 256 is a continuation of one of the sub-paths 219A-H, and path 257 is a continuation of one of the sub-paths 224A-H. In this example, path 256 continues sub-path 219H and path 257 continues sub-path 224A. Sub-paths 219H and 224A may and are expected to differ in length. To assure that component clock signals 218 and 222 have the same phase at the respective registers, paths 256 and 257 should be equal in length and have the same or similar propagation delay characteristics. A factor determining propagation delay difference is the difference between the lengths of the paths. In a preferred embodiment, the difference between propagation delay of length of paths 256 and 257 is less than 15%.

Paths 256 and 257 couple their respective components to phase feedback element 255. Phase feedback element 255 determines the phase difference between component clock signals 218 and 222, and generates an adjustment signal 267, which is provided to clock driver 220 in either analog or digital form (analog skew or digital skew values). Adjustment signal 267 is a measure of an advance or delay that allows component clock signal 222 to become in phase with component clock signal 218. An adjusted clock signal 222 may then be used as a "reference clock" signal for other component clock signals.

In a similar manner, phase feedback element 260 receives component clock signal 222 from path 261, and component clock signal 227 from path 262. Path 261 is a continuation of one of the sub-paths 224A-H, and path 262 is a continuation of one of the sub-paths 229A-H. In this example, path 261 continues sub-path 224H and path 262 continues sub-path 229A. Sub-paths 224H and 229A

may and are expected to differ in length. To assure that component clock signals 222 and 227 have the same phase at the respective registers, paths 261 and 262 should be equal in length and have the same propagation delay characteristics.

Paths 261 and 262 couple their respective components to phase feedback element 260. In this example, phase feedback element 260 corresponds to the adjacent pair of components 200 and 205. Phase feedback element 260 determines the phase difference between component clock signals 218 and 222, and generates an adjustment signal 277 which is provided to clock driver 225 in either analog or digital form (analog skew or digital skew values). Adjustment signal 277 is a measure of an advance or delay that allows component clock signal 227 to become in phase with component clock signal 222. Since component clock signal 222 has been adjusted to match the phase of component clock signal 218, it follows that component clock signal 227 is adjusted to match the phase of component clock signal 218.

Although this example describes synchronization of component clock signals from a left to right sequence beginning with a left most component, it is contemplated that synchronization may start with any component clock signal, including a component clock signal received at a middle component (byte-word register) or middle bit register.

Fig. 3 illustrates an exemplary embodiment of phase feedback element 255. Phase feedback element 260 is similarly implemented. This implementation of feedback element 255 is particularly appropriate in circuits where components or registers have 10 or fewer bits.

Phase feedback element 250 includes a phase comparator 305. Phase comparator 305 receives component clock signals from a pair of components;

allowing the phase feedback element to adjust the phase of one of the component clock signals to match that of the other component clock signal. In particular examples, the phase comparator 305 receives a clock signal from a first bit register of a plurality of bit registers in a component and a clock signal from a last bit register of a plurality of bit registers in a second component. The clock signals from these bit registers may be routed through paths that have matched lengths. In this example, phase comparator 305 receives component clock signals 218 and 222, and determines the phase difference between component clock signals 218 and 222. Phase comparator 305 may include a phase converter that converts the phase difference to a phase offset value or digital skew time value 310. Digital phase offset value or digital skew time value 310 may be stored in a clock register 315. Based on digital phase offset value or digital skew time value 310, clock register 315 instructs clock driver 220 to advance or delay transmission of component clock signal 222. Digital phase offset value or digital skew time value 310 is used as adjustment value 267 of Fig. 2.

Referring now to Fig. 4, illustrated is an exemplary embodiment of a phase feedback element 255 using current sources. Phase feedback element 260 is similarly implemented. This implementation is particularly appropriate in circuits having more than 10 bits in each component or register.

In this embodiment, phase feedback element 255 has an integrator or capacitance 405 and current sources 415 and 420. Current sources 415 and 420 are controlled by switches 425 and 430, respectively. Current source 415 corresponds to component 200 and current source 420 corresponds to component 205, where in this example components 200 and 205 are treated as a pair. Switches 425 and 430 are preferably implemented as transistors. Current sources

415 are connected through the respective switches 425 and 430 to charge and discharge capacitance 405. Specifically, current source 415 is connected through and enabled by switch 425 to charge capacitance 405 when switch 425 is closed. Current source 420 is connected through and enabled by switch 430 to discharge capacitance 405 when switch 430 is closed. Current sources 415 and 420 preferably source equal currents, albeit in opposite directions. In other words, current sources 415 and 420 are matched current sources.

Switches 425 and 430 are selectively enabled or controlled by the component clock signals of the two adjacent components corresponding to phase feedback element 255, in this case by component clock signals 218 and 222. Switch 425 is closed when component clock signal 218 is logically true or high, and is open when component clock signal 218 is logically false or low. Switch 430 is closed when component clock signal 222 is logically true or high and is open when component clock signal 222 is logically false or low. If the component clock signals 218 and 222 are in phase, switches 425 and 430 close and open at the same times, and the net effect of the opposite current sources 415 and 420 is null—the capacitance 405 is neither charged nor discharged.

If, on the other hand, component clock signals 218 and 222 are out of phase, switches 425 and 430 do not close and open at the same times, and there is a net charging or discharging effect on capacitance 405. Assuming a relatively large capacitance 405, the voltage at the capacitance will increase or decrease, relative to ground, in accordance with any phase difference between the two component clock signals 218 and 222. Thus, the voltage at capacitive node 435 represents a phase difference between component clock signals 218 and 222. In the illustrated embodiment, phase feedback element 255 has an analog to digital

(A/D) converter 440 that converts the analog skew or voltage value at capacitive node 435 to a digital skew time value 445. Clock driver 220 advances or delays component clock signal 222 based on digital skew time value 445. Clock driver 220 therefore is responsive to the voltage value at capacitive node 435. In other embodiments, analog skew value 435 is passed directly on to clock driver 220.

Although details of specific implementations and embodiments are described above, such details are intended to satisfy statutory disclosure obligations rather than to limit the scope of the following claims. Thus, the invention as defined by the claims is not limited to the specific features described above. Rather, the invention is claimed in any of its forms or modifications that fall within the proper scope of the appended claims, appropriately interpreted in accordance with the doctrine of equivalents.